NONVOLATILE SWITCH, IN PARTICULAR FOR HIGH-DENSITY NONVOLATILE PROGRAMMABLE-LOGIC DEVICES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a nonvolatile switch, in particular for high-density nonvolatile programmable-logic devices.

Description of the Related Art

As known, programmable-logic devices are currently mainly formed by RAMs, which must be written each time the device is turned on. It is therefore necessary to provide an external memory that contains the code to be loaded at turning-on.

To eliminate the above need, programmable-logic devices, based upon nonvolatile components, have already been proposed. A solution is disclosed in US-A-5 015 885, wherein a nonvolatile cell (EPROM or EEPROM) operates directly as a switch for connecting or separating horizontal and vertical segments formed by pass transistors. However, this solution is problematical as regards management of the switches, since they carry out two different functions and hence require a separate encoding for each function.

In other solutions, disclosed for example in US-A-6 625 221 and US-A-5 576 568, a floating strip of polysilicon forming the gate electrode of a pass transistor is prolonged and used as the first plate of a capacitor, the second plate whereof is connected to a terminal of a coupling transistor. The polysilicon strip moreover forms the floating gate of an EEPROM cell or a plate of a further coupling capacitor to enable injection or extraction of charges from the polysilicon strip and hence programming and erasing of the cell. Also, these solutions are disadvantageous, since they require a large area and cannot be integrated in a

memory array. Programming of the cells moreover requires high voltages, which are hardly from compatible with the devices and circuits integrated in the same chip.

BRIEF SUMMARY OF THE INVENTION

The aim of the present invention is thus to provide a nonvolatile switch overcoming the drawbacks indicated above.

According to the present invention, a nonvolatile switch and a method for controlling a nonvolatile switch are provided, as defined in claim 1 and 9, respectively.

According to one aspect of the present invention, the switch is formed by a flash cell and a pass transistor, which have a common floating-gate region. The flash cell enables modification of the charges contained in the floating-gate region by channel hot-electron injection (writing) and extraction by Fowler-Nordheim (FN) tunneling effect (erasing), and hence modulation of the threshold of the pass transistor. The pass transistor therefore has a variable threshold, which depends upon the charge present in the floating-gate region. The flash cell and the pass transistor also share the control-gate region. The pass transistor is connected to the outside of the cell and enables or not passage of the logic signals from the input terminal to the output terminal according to the threshold programmed. If the threshold of the pass transistor is sufficiently low, once it has been selected through its control gate region, it outputs the logic signal present at input. If, instead, the threshold of the pass transistor is high, it is off even when it is selected and does not enable passage of the logic signal.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

For an understanding of the present invention there are now described some preferred embodiments thereof, which are provided purely by way of non-limiting example, with reference to the attached drawings, wherein:

Figure 1 illustrates the equivalent electrical circuit of a switch according to a first embodiment of the invention;

Figure 2 shows the layout of a first implementation of the switch of Figure 1;

Figure 3 is a cross-section taken along line III-III of Figure 2;

Figure 4 is the layout of a second implementation of the switch of Figure 1;

Figure 5 illustrates the equivalent electrical circuit of a second embodiment of the switch according to the invention;

Figure 6 is the layout of an implementation of the switch of Figure 5; and

Figure 7 is a table corresponding to the biasings supplied to the switch according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows a switch 1 comprising a memory element 2, of a flash type, and a pass transistor 3, which have a same floating-gate region 4 and a same control-gate region 5. In practice, the memory element 2 and the pass transistor 3 share the gate regions 4, 5.

In detail, the memory element 2 has a drain terminal FD connected to a first bias generator 10 and a source terminal FS connected to a second bias generator 11. The pass transistor 3 has a drain terminal PD connected to a data input 12 and a source terminal PS connected to a data output 13. In addition, the control-gate region 5 is connected by a terminal CG to a third bias generator 14, and a body region B, in common both to the memory element 2 and to the pass transistor 3, is connected to a fourth generator 15.

The table of Figure 7 illustrates by way of example the biasings supplied to the terminals FD, FS, PD, PS, CG, and B in the different operating conditions of the switch 1. In particular, the table shows the biasing conditions

during writing of the memory element 2, by channel hot-electron injection, and during erasing, by FN tunneling effect, when suitable voltages are applied to the drain terminal FD, source terminal FS, floating-gate terminal CG, and body terminal B, while the pass transistor is inoperative and its terminals PS and PD are floating. Instead, during turning on and off of the switch, the drain terminal of the memory element 2 is maintained floating, the source terminal is grounded, and the digital datum (bits 0 or 1, with a voltage linked to the technology used) is supplied at the input 12 of the pass transistor 3. As indicated, if the memory element 2 is erased, the threshold voltage of the pass transistor 3 is low, and the digital datum can be supplied on its output 13. Instead, if the memory element 2 is written, the threshold of the pass transistor 3 is high, and the digital datum is not supplied on the output 13.

The table of Figure 7 also indicates the biasings that enable reading of the memory element 2 for verifying the set threshold.

The switch 1 can be implemented in a very compact way, as is illustrated by way of example in the layout of Figure 2 and in the cross-section of Figure 3.

In particular, in the illustrated embodiment, the memory element 2 is made in a first active area 20, and the pass transistor 3 is made in a second and a third active areas 21, 22. The active areas 20-22 extend parallel to one another in a well region 24 (see Figure 3) of semiconductor material and are electrically separated from one another by field-oxide regions 25.

On top of the well 24, there extend, in order (see Figure 3): a gate oxide layer 26; the floating gate region 4; an interpoly dielectric layer 27; the control gate region 5; and a top dielectric region 28. The top dielectric region, formed by various layers, accommodates a pass source connection line 30, a pass drain connection line 31, a memory source connection line 32, and a memory drain connection line 33, all formed in a same metal layer (metal I).

As may be noted in Figure 2, the pass source connection line 30 is connected to pass source regions 35, 36 formed in the second active area 21 and the third active area 32, through a first contact 37 and a source local-interconnection line (LIL) 38, formed directly on top of the substrate 24 between the pass source regions 35 and 36. Likewise, the pass drain connection line 31 is connected to pass drain regions 40, 41 formed in the second active area 21 and the third active area 22, through a second contact 42 and a drain local-interconnection line 43, formed directly on top of the substrate 24 between the pass drain regions 40 and 41.

In practice, the pass transistor 3 comprises two pass transistors formed in two adjacent active areas (second and third active area 21, 22) and parallel-connected so as to operate as a single pass transistor 3 with an area sufficient to conduct the required current.

In addition, the memory source connection line 32 is connected to a memory source region 45 formed in the first active area 20, through a third contact 46. Instead, the memory drain connection line 33 is connected to a memory drain region 47 formed in the first active area 20, through a fourth contact 48 and a memory local-interconnection line 50, formed directly on top of the substrate 24 between the memory drain region 47 and the fourth contact 48.

Figure 4 illustrates a variant of the layout of Figure 2, wherein the pass transistor 3 is formed in a single active area 60 corresponding to the area of the second and third active areas 21, 22 and of the intermediate field oxide region 25 of Figure 2. Consequently, just one pass source region 61 is connected to the pass source connection line 30 only through a first contact 37, and one pass drain region 62 is connected to the pass drain connection line 30 though the second contact 42.

Figure 5 illustrates the electric diagram of a different embodiment, wherein a same memory element 2 is associated to more pass transistors, here two pass transistors 3a, 3b, so as to form a multiple switch 1'.

Analogously to what illustrated in Figure 1, the pass transistors 3a, 3b share the floating-gate region 4 and control-gate region 5. Each pass transistor moreover has a drain terminal PDa, PDb connected to a respective data input 12a, 12b and a source terminal Psa, PSb connected to a respective data output 13a, 13b.

This solution proves advantageous when the pass transistors are to be configured in the same way and selected simultaneously (for example, for connection to a bus), thanks to the saving in the occupied area that can be obtained.

Also, the above embodiment enables different embodiments of the layout. For example, the four active areas forming the pass transistors 3a, 3b can be joined in pairs, as illustrated in Figure 4.

Thanks to the described structure, it is possible to obtain a nonvolatile switch with an extremely reduced area. In addition, the described switches can be made using standard technology for manufacturing flash cells, and hence using machines commonly available in the microelectronics industry and known and reliable processing steps. The use of a flash memory element further enables also negative voltages to be used, with a consequent reduction of the amplitude of the voltages applied.

In addition, it is possible to form the switch within a flash-memory array, and hence in a still more compact way. In this case, the connection lines 30-33 operate as bitlines, and the control-gate region 5 operates as a wordline.

Finally, it is clear that numerous modifications and variations can be made to switch described and illustrated herein, all of which fall within the scope of the invention, as defined in the attached claims. For example, also the memory element 2 can be formed in two distinct active areas, and the floating gate region can be shortened so as to end above the first active area 20 (see Figure 3). In addition, since the pass transistor 3 is a symmetrical element, the data input 12

and the data output 13 can be connected to the drain terminal PD and the source terminal PS in an opposite way with respect to what is illustrated.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.